REMARKS

The Request For Continued Examination (RCE) Transmittal submitted in the above-identified application, concurrently herewith, is noted. This RCE Transmittal is responsive to the Final Office Action mailed June 4, 2002, and the present amendments act as the necessary Submission in connection with the RCE Transmittal. Granting of the Request For Continued Examination, and entry of the present amendments, in due course, are respectfully requested.

By the present amendments, Applicants are adding new claims 60-83 to the application. Claim 60, dependent on claim 1, recites that the Sn-Bi alloy layer is directly in contact with the lead or directly in contact with a Cu layer in contact with the lead, and the Pb-free solder is directly in contact with the Sn-Bi alloy layer. Claim 61, dependent on claim 60, recites that the Pb-free solder is also directly in contact with the substrate. In connection with claims 60 and 61, note, for example, Figs. I and 2 of Applicants' original disclosure. Claims 62-77 correspond to either claim 60 or claim 61, but are dependent on others of the independent claims in the application (that is, claims 6, 11, 19, 24, 43, 50, 51 and 59).

New independent claim 78 defines an electronic device including a semiconductor device having an electrode structure which includes a lead and a Sn-Bi alloy layer containing 1-5 wt% Bi which is formed directly on the lead, and a circuit board connected to the semiconductor device with a solder made of a Pb-free alloy, the connection being formed by contacting and soldering the alloy layer and the solder. Claims 79 and 80, each dependent on claim 78, further defines the Pb-free solder; and claims 81 and 82, each dependent on claim 78, respectively recites that the connection includes tin, silver, bismuth and copper; and that the lead is made of

an iron-nickel alloy, and a copper layer is provided between the lead and the alloy layer.

New independent claim 83 defines an electronic device including a semiconductor device and a circuit board as in claim 78, the circuit board being connected to the semiconductor device, and further recites that the connection between the semiconductor device and the circuit board is formed by soldering during which the solder is initially in contact with the tin-bismuth alloy and subsequently melted, whereby the tin-bismuth alloy is melted and mixed with the solder under heat from the solder.

Applicants respectfully traverse the rejection of their claims as set forth in the Office Action mailed June 4, 2002, especially in light of the following comments.

That is, it is respectfully submitted the teachings of the reference applied in the Office Action mailed June 4, 2002, that is, U.S. Patent No. 6,110,608 to Tanimoto, et al, would have neither taught nor would have suggested such an electronic device as in the present claims, including, inter alia, the structures (including a lead on the semiconductor device) connected with each other by means of a lead-free solder, with the lead having a tin-bismuth alloy layer including 1-5 wt% Bi is formed as a surface layer.

As will be developed more fully in the following, it is respectfully submitted that the teachings of Tanimoto et al the applied prior art would have neither disclosed nor would have suggested the connection including the lead-free solder, the teachings of Tanimoto, et al. not including a solder layer.

Furthermore, it is respectfully submitted that this reference would have neither disclosed nor would have suggested such an electronic device as in the present

claims, including the direct contact between various of the structures, or wherein one of the structures is "directly formed on", or directly on", another of the recited structures. In connection therewith, note, in particular, claims 6, 11, 19, 24 and 60-83, for example.

More particularly, this applied reference would not have taught, nor would have suggested, such electronic device as in the present claims, wherein the tin-bismuth alloy layer is directly in contact with the lead or directly in contact with a copper layer in contact with the lead, and the lead-free solder is directly in contact with the tin-bismuth alloy layer (note, for example, claim 60 and corresponding claims dependent on other independent claims); and/or wherein, additionally, the lead-free solder is also directly in contact with the substrate (note, for example, claim 61 and corresponding claims dependent on other claims).

The invention as claimed in the above-identified application is directed to an electronic device utilizing a lead-free solder to connect a lead electrode structure of a semiconductor device and a substrate (for example, an electrode on a circuit board). Applicants have found that by using a tin-bismuth plating layer having 1-5 wt% bismuth, on the lead of the semiconductor device, as a surface layer, or on a copper layer on the lead, good wettability of the lead-free solder and a high bond strength are achieved, while avoiding whisker formation. As to advantageous effects achieved according to the present invention, note, for example, Figs. 4-7 of Applicants' disclosure, showing advantages achieved by the present invention in strength and wettability. Such advantageous effects as shown in Applicants' disclosure must be considered in a determination of unexpectedly better results achieved by the present invention. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984). It is respectfully submitted that these advantageous results achieved according to the present

invention show unexpectedly better results achieved according to the present invention, and further establishes unobviousness of the present invention.

The present invention is directed to an electronic device having a soldered bond, as compared with, for example, a weld bond, for connection of the semiconductor device and the substrate. The present inventors directed their attention to the problem of reliability in bonding, in the case where a lead-free solder is used for bonding; and, based on results of experimentation, have found that advantageous results in the soldered bond are achieved when the bismuth content of a tin-bismuth alloy layer, on a lead bonded with the solder, is 1-5 wt%.

That is, as described particularly on pages 5 and 6 of the specification of the above-identified application, a soldered connection of an electronic device, of a lead-free solder, is achievable using a tin-bismuth alloy layer having 1-5 wt. % Bi on the lead, particularly when a tin-silver-bismuth alloy layer is used as the solder. Moreover, the bonded (soldered) structure formed has high strength and a stable bond interface, and has good resistance to occurrence of whiskers. In addition, the tin-bismuth solder layer with 1-5 wt% bismuth has good wettability. Thus, it is possible to obtain an interface having good bonding strength and wettability sufficient for practical use, and there is good resistance to formation of whiskers, so that it is possible to realize lead-free electronic devices which are environmentally friendly.

Tanimoto, et al discloses a lead material for an electronic part, a lead and a semiconductor device using the same. The lead material is one in which the surface of a conductive substrate is coated with a plated layer made of a tin group of material which does not contain Pb, so that the lead material does not give an adverse influence to the environment because it does not contain Pb, and it also has excellent solderability (or solder wettability) and provides a strong junction with a

solder, and does not cause non-uniform thickness of the plated layer even in reflow processing. The described structure has a lead material with a first plated layer and a second plated layer provided on a surface of a conductive substrate in this order, a melting temperature of the material of the second plated layer being lower than that of a material of the first plated layer. See column 2, lines 43-49. This patent discloses that the lead material for the electronic part can include a first plated layer made of a Sn substance and a second plated layer made of a Sn alloy containing at least one element selected from a group of Ag, Bi, Cu, In and Zn; or, alternatively, the first plated layer can be made of a Sn alloy containing at least one element selected from a group of Ag, Cu, Sb and Y and a second plated layer made of a Sn substance. See column 2, lines 50-60. As to the Sn-Bi alloy, this patent discloses that the Bi percentage content can be up to 87 wt%. See column 4, lines 23-27. However, this patent further discloses that if the lead material provides a junction with a solder and 20 wt% or more Bi exists at the solder part, the junction strength of the solder part gradually deteriorates, so that the alloy composition is preferably adjusted such that the Bi percentage content at the junction part after soldering is 20 wt% or less. This patent further discloses that an Sn-Bi alloy having a Bi content of 30 wt% or less as the Sn alloy is generally preferred. See column 4, lines 48-62.

Tanimoto, et al is directed to a problem when a single plating layer of a lead-free material (for example, tin-bismuth) is formed on a conductive substrate, taking into account the environment, and in order to solve this problem, proposes to provide a lead material in which a first lead-free plating layer and a second plating layer are formed on the substrate, the melting temperature of the second plating layer being lower than that of the first lead-free plating layer.

In addition to previous arguments made in, for example, the Amendment filed March 18, 2002, it is respectfully submitted that the teachings of Tanimoto, et al would have neither taught nor would have suggested the lead-free solder for the connection, particularly using the specific tin-bismuth alloy as the alloy layer with the lead-free solder as in the present claims, and advantages achieved thereby. That is, it is emphasized that Tanimoto, et al is silent with respect to use of a Pb-free solder, with the lead material having the first and second plated layers without disclosure of a Pb-free solder.

In this regard, the contention by the Examiner in Item II on page 7 of the Office Action mailed June 4, 2002, that the discussion in Tanimoto, et al of tin alloys with a higher bismuth content concerns the lower melting point second layer "that functions as the lead free solder" is respectfully traversed. It is respectfully submitted that the second layer in Tanimoto et al. forms part of the lead, and is not a Pb-free solder material. In this regard, note that Tanimoto, et al discloses test results exhibiting reliability in bonding the lead material with use of eutectic solders; such eutectic solders containing Pb. See, for example, column 7, lines 52-57 of Tanimoto, et al. In addition, note that the second plating layer in Tables 1-3 of Tanimoto, et al, has a thickness of 0.5-12 pm, and that it is technically impossible to solder a lead material to a substrate by means of a plated layer having such a thin thickness of 0.5-12 pm. Thus, contrary to the contention by the Examiner, it is respectfully submitted that Tanimoto, et al discloses a lead structure with two layers, used together with an additional layer for welding or soldering (that is, an additional layer such is, ~ the solder layer), and would have neither taught nor would have suggested the presently claimed subject matter, including the, for example, single

layer of tin-bismuth with specified amount of bismuth between the lead and Pb-free solder, and advantages thereof as discussed in the foregoing.

It is emphasized that the lead material of Tanimoto, et al has a conductive substrate with first and second plating layers in sequence on the substrate. It is respectfully submitted that the second plating layer has a lower melting point than that of the first plating layer, so that the first plating layer serves as a barrier layer for preventing diffusion of copper from the conductive substrate during soldering (note, for example, column 3, lines 44-47 of Tanimoto, et al). However, it is respectfully submitted that the lead material of Tanimoto, et al has the following problems. The bonding strength is low because an insufficient amount of intermetallic compound is formed between the first plating layer (which is not melted) and the conductive substrate. Furthermore, in a case where the first plating layer has a different chemical composition from the second plating layer, or where the first plating layer is different from the second plating layer in bismuth content, there arises a problem of non-uniform chemical composition in a bonding solder after the reflow-soldering process; and, thereafter, during use of a semiconductor device with a lead material as in Tanimoto, et al, there will occur diffusion between the first plating layer and the bond solder so as to dissolve the non-uniformity of the chemical composition, resulting in that the bonding solder structure changing gradually in chemical composition, so that stability and reliability of the connection changes. In addition, in the case of the first plating layer of tin being provided on the second plating layer of tin-bismuth, there also arises a problem of occurrence of whiskers. In addition, and as can be appreciated from the manufacturing process, by use of the two plating layers the number of production process steps is increased and production cost also increases.

In contrast, according to the present invention utilizing the tin-bismuth alloy layer with relatively small amount of bismuth, and the lead-free solder, the foregoing problems in connection with use of the two plating layers can be avoided.

In addition, attention is also directed to those of the present claims which further include a copper layer between the lead substrate and the tin-bismuth layer. An advantage of this structure, which has an intermediate layer of copper, is described on pages 13-15 of Applicants' specification. It is respectfully submitted that Tanimoto, et al does not disclose, nor would have suggested, the presently claimed subject matter including the copper layer, or advantages thereof as in the present invention.

The undersigned notes the interview which the Examiner has courteously granted to the undersigned in connection with the above-identified application and the parent application thereof, on November 6, 2002. It is respectfully requested that the Examiner hold off examination of the above-identified application in response to the concurrently filed Request For Continued Examination and the present Submission (Amendment), until after the above-mentioned interview.

Withdrawal of the finality of the Office Action mailed June 4, 2002, based upon granting of the Request for Continued Examination, entry of the present amendments, and further examination of the above-identified application after conducting of the above-mentioned interview, are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135

(Case No. 500.38665CX1), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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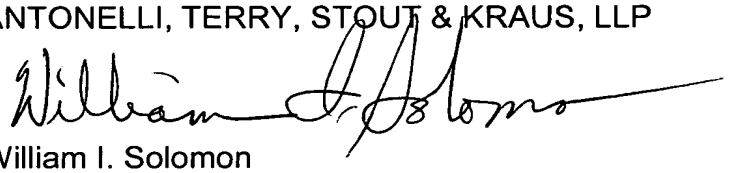

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